ABSTRACT OF THE DISCLOSURE

Disclosed is a circuit for controlling the duty cycle and jitter of a clock signal. The circuit has an input node for receiving the clock signal and an output node for outputting a processed clock signal having a first edge that is synchronized to an edge of the clock signal and a second edge that is varied so as to provide a predetermined processed clock signal duty cycle. The predetermined duty cycle is preferably a 50-50 duty cycle. The output node may be coupled to baseband circuitry of a wireless communications terminal, such as a cellular telephone. The circuit is constructed to include a plurality of serially connected delay elements that are coupled to the clock signal at the input node. The plurality of delay elements together introduce a nominal one cycle delay into the clock signal. The circuit also includes a phase detector having a first input signal coupled to the clock signal and a second input coupled to an output of the plurality of delay elements for receiving a delayed clock signal therefrom. The phase detector operates so as to generate an error signal that is indicative of a phase difference between the clock signal and the delayed clock signal. The error signal is coupled to at least one of the delay elements for controlling the delay element for minimizing the phase difference between the clock signal and the delayed clock signal. The circuit also includes a first divider circuit having an input coupled to the clock signal, a second divider circuit having an input coupled to an output of a first one of the plurality of delay elements for receiving a one half cycle delayed clock signal therefrom, and a gate having inputs coupled to outputs of the first and second divider circuits and an output coupled to the output node for outputting the processed clock signal.